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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/684,868	10/06/2000	Zhaohui Shen	00-255 1496.00039	2832
24319	7590	11/04/2003	EXAMINER	
LSI LOGIC CORPORATION 1621 BARBER LANE MS: D-106 LEGAL MILPITAS, CA 95035			DINH, PAUL	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/684,868

Applicant(s)

SHEN ET AL.

Examiner

Paul Dinh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 September 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,4-9 and 11-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,4-9 and 11-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 06 October 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

*Detailed Action.*

This is a response to the amendment/remarks filed on 9/29/03. The amendment does not overcome prior art; therefore,

The previous reference(s)/rejections are retained and repeated; and  
New grounds of rejections have been cited in this office action in view of the amendment.  
See the following details.

*Drawings*

I the drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

- a. New claim 32 recites “internal state machines” feature; therefore, this feature must be clearly shown/labeled in the drawings or this feature canceled from the claim.
- b. Claim 1 recites a “functional portion”; therefore, the “functional portion” must be clearly labeled in the drawings or the “functional portion” canceled from the claim. The applicant states in remarks page 9 that “**figure 2 illustrates an example of a functional portion with the FPGA core 116**”. It is still not clear that the applicant means: “a functional portion” is the FPGA core 116 or “a functional portion” **within** the FPGA core 116 or “a functional portion” is a separate entity from the FPGA core 116.

**Clarification is required and the “functional portion” must be clearly labeled in figure 2.**

II The drawings filed on 10-6-00 are subject to correction of the informalities indicated on the attached “Notice of Draftsperson’s Patent Drawing Review,” PTO-948 (mailed 6/27/03). In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

*Claims Objections*

The following claims are objected to because:

(Claim 1) it is not clear **what being “configured”**; the functional portion being configured or the logic portion being configured or both functional portion and logic portion being configured.

(Claim 1) “said FPGA core” lacks antecedent basis.

(Claim 22) improper dependency (depends on a cancelled claim)

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(Claims 26, 28) "N" is not clearly described in the specification and claim(s), see 37 CFR 1.75 (d)

(Claim 32) "the active time", "the internal state machines", and "the execution average" lack antecedent basis.

(Claim 33) "the specific values" and "the host register values" lack antecedent basis,

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

*A person shall be entitled to a patent unless –  
(e) The invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.  
The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).*

Claims 1, 4-9, 11-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Killian et al (USP 6477683) who discloses a system/method comprising:

(Claim 1)

a functional portion and a logic portion connected to said functional portion and configured to detect, fix errors or verify fixes of errors in said functional portion (fig 1-3, 5-15), wherein said logic portion includes one or more interfaces;

*(Interfaces/connection interfaces/host interface/bus I/F/development I/F/communication I/F/link I/F as shown in fig 1-3, 5-15 and/or data /lines/address /lines/Input/output bus/lines/ processor I/F/ pins/port/buffers/drivers/software I/F/hardware I/F/control bus/lines/input/output Interface in fig 1-3, 5-15/ configuration I/F (20 of fig 1, 100 of fig 6)/processor I/F (70 of fig 2)/Graphic user I/F (fig 3-4)/ / c31: 31-39 (ISS 126 provides several interface/socket I/F)/memory I/F/register I/F in fig 1-3, 5-15/etc)*

a debugging/bug fix circuit (abstract/c1-4, 6/on-chip debug module 92 in fig 2) configured to detect errors in said logic portion through said one or more interfaces; and

diagnostic architecture using [said] an FPGA core (c32: 54, c33: 2, c34) in system on a chip design (on-chip debug module 92 in fig 2/c2: 2-3/c7: 32-35/c12: 3-37/claim 65 (processor on a chip)))

(Claim 4) said system is configured to provide ease in bringing up (this is merely an intended used and/or expected result, just for applicant information the prior art teach intended use/expected result in c11: 14+(bringing up)), verification (abstract/background/summary) and debugging (abstract/background/summary, also see fig 1- 2, 6), each by interconnecting said circuit and said debugging/bug fix circuit (fig 1-15)

(Claim 5) said system is configured to provided one or more programming options for said circuit (background/summary and/or, see flexibility/options/changes/variety/differences in code/software/programs/instructions/algorithms/tools/design/configuration in this prior art)

(Claim 6) observation of one or more signals by said debugging/bug fix circuit (fig 1-15)

(Claims 7-8) observation of one or more signals when running in a normal mode (c13: 22), single step mode (c24: 8+, c25: 63, c29: 48)

(Claims 9, 11) single step mode when control by a gate or core, said core comprises an FPGA core, said core is programmable (fig 1-2, 6-15, c32-33)

(Claim 12) debugging workstation (debugging computer/system/platform in fig 1/c30: 20+, c31: 11+, c32: 34+)

(Claims 13, 22) said debugging/bug fix circuit (and said circuit) is/are further configured to allow or more debugging features (fig 1-8 and/or c29-32)

(Claim 14) triggering and tracing based on one or more signals (c12-13, fig 2, 8)

(Claim 15) dynamically changing host register values (fig 1, c5 and/or c13-16 and/or c30-31)

(Claim 16) complex monitoring function (c2, 21)

(Claim 17) configured to reduce the debugging/verification time and/or improved product time to market is merely and intended use and/or expected result; just for the applicant information, this prior art also teach intended use and/or expected result; i.e., abstract, field of invention and/or c2, 32, 35)

(Claim 18) said circuit is further configured to operate in a normal mode (c13: 22) and a single step mode (c24: 8+, c25: 63, c29: 48)

(Claim 19) said normal mode is configured to allow said circuit to present one or more internal signals of said functional portion and said single step mode in configured to provide a plurality of signals of said functional portion (fig 1-15)

(Claim 20) Scan chain is used to diagnose or fix a bug via the logic portion (c12, 21, 29, 43 and/or fig 9-15)

(Claim 21) the logic portion is further configured to bridge one or more of said plurality of signals between a plurality of modules (fig 1-2, 6, 8)

(Claim 23) CAD software to provide one or more diagnostic functions (fig 1/42 and/or c12 and/or debugging/diagnostic softwares/programs/CADs/tools as taught in this reference)

(Claim 24) diagnostic function are selected from the group consisting of searching for a specific signal pattern, tracing the internal state machine, triggering on a programmed condition, and other appropriate diagnostic functions (fig 2, 6, 8 and/or c3, 5, 13, 19-20, 27, 33-34)

(Claim 25) diagnostic function are selected from the group consisting of on the fly monitoring of a correctness of a bus protocol, and implement statistics counting to measure the performance and the testing coverage (fig 2, 6, 8 and/or c2-4, 19-20, 23, 27, 33-34, 41-42)

(Claim 26)

(A) interfacing a chip with [a] an FPGA core (c32: 54, c33: 2+, fig 1-15)

(B) presenting one or more internal signals of said chip (fig 1-15)

(C) verifying or fixing bugs in said chip with said one or more internal signals  
(abstract/background/fig 1-15); and

(D) programming the FPGA core to dump data from a host register every N clock cycles.

*(The feature in step (D) is taught in c20: 13+, c31: 39+ and/or the limitation in step (D) implemented by on chip programming of the FPGA and debugging software/program as taught in c2: 2-3, c7: 33+, on-chip debug module 92 in fig 2/software debug in fig 6/c11-13/c30: 38+, c25: 64-c25: 7, c29: 62-c32)*

(Claim 27) a computer readable medium configured to store instruction for executing the steps of claim 26 (fig 1 and/or c12: 31+, c26: 1-2, c30: 20+, c31: 11+, c32: 34+)

(Claim 28) capturing signals every N clock cycles

*(Fig 1-15 and/or implemented by a combination of on chip programming/configuration of the FPGA and debugging software/program as taught in c2: 2-3, c7: 33+, on-chip debug module 92 in fig 2/software debug in fig 6/c11-13/c30: 38+, c25: 64-c25: 7, c29: 62-c32)*

(Claim 29) dynamically changing the values in said host register

*(Fig 1, c5/c13-16/20/c30-32 and/or implemented by on chip programming/configuration of the FPGA and debugging software/program as taught in c2: 2-3, c7: 33+, on-chip debug module 92 in fig 2/software debug in fig 6/c11-13/c16: 16+/c30: 38+, c25: 64-c25: 7, c29: 62-c32)*

(Claim 30) searching for a specific signal pattern (fig 6-15/c19/c35: 43)

(Claim 31) monitoring the correctness of a bus protocol (fig 1-15 and c2: 35-c3: 2, c29: 55-65, c34: 34+)

(Claim 32) implement statistics counting to measure: [the] an active time on bus request and [the] an execution average of [the] internal state machines (c27, 33-34, fig 2, 6-8)

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(Claim 33) triggering and tracing based on internal signals (fig 2, 8); triggering based on [the] specific values of address, data, or command bus (fig 2-15); dynamically changing [the] host register values (fig 1, c5/c13-16/20/c30-32 and/or *on chip programming of the FPGA and debugging software/program as taught in c2: 2-3, c7: 33+, on-chip debug module 92 in fig 2/software debug in fig 6/c11-13/c16: 16+/c30: 38+, c25: 64-c25: 7, c29: 62-c32*); and monitoring protocol bus function (fig 6 and/or c2: 35-c3: 2, c29: 55-65, c34: 34+)

### Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is (703) 305-5662. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (703) 308-1323. The fax number for the organization handling this application is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Paul Dinh

Patent Examiner



LEIGH M. GARBOWSKI  
PRIMARY EXAMINER